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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,772	11/21/2003	Leonard Forbes	400.252US01	2900

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,772	FORBES, LEONARD	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6-21* is/are rejected.

7)☒ Claim(s) *2, 5, 7 and 22-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 4, 6, 11, 13-17, 19-21, are rejected under 35 U.S.C. 102(e) as being anticipated by Yuan et al. (U.S. Patent No. 6,762,092 B2).

In re claim 1, Yuan (esp. Fig. 25A) discloses a semiconductor memory device comprising:

A plurality of oxide pillars (407) each having a source/drain region (449, 451), a trench being formed between each pair of oxide pillars;

A control gate (411) formed between each pair of oxide pillars;

A plurality of program (steering) gates (412), each formed between the control gate and each oxide pillar, each program gate extending along the oxide pillar sidewall; and

A plurality of gate insulator layers (406, ONO), each gate insulator layer formed between each program gate and the adjacent oxide pillar, each gate insulator layer having a structure for trapping at least one charge.

In re claim 3, Yuan discloses the device of claim 1, wherein the plurality of gate insulators are comprised of a composite ONO structure such that the nitride [is] the charge trapping structure.

In re claim 4, Yuan discloses the device of claim 1, and further including a silicon oxide (oxide portion of 406) gate insulator formed between the control gate and the adjacent program gates and along the bottom of the trench.

In re claim 6, Yuan discloses the device of claim 1, wherein each gate insulator layer comprises silicon oxide. The phrase, "formed by wet oxidation and not annealed" is a product-by-process limitation that does not further distinguish the final structure of the claimed invention from the prior art.

In re claims 11, 14, 17 and 21, Yuan (Fig. 25A-26A) discloses a method and an array of semiconductor memory devices comprising:

A plurality of oxide pillars (407) each having a source/drain region (449, 451) formed at the top, a trench being formed between each pair of oxide pillars;

A plurality of control gates (411), each control gate formed in the trench between each pair of oxide pillars;

A plurality of program gates (412), each formed in the trench between a first control gate and each oxide pillar, each program gate extending along the oxide pillar sidewall;

A plurality of gate insulator layers (406), each gate insulator layer formed between each program gate and the adjacent oxide pillar, each gate insulator layer having a structure for trapping at least one charge (ONO); and

A word line (492 coupling the plurality of control gates.

Yuan does not expressly disclose a CPU coupled to the array of memory cells, but inherency dictates that this memory array will be used in some type of device that has central processing characteristics.

In re claim 13, Yuan discloses the device of claim 11, wherein each source/drain region is comprised of an n-type conductivity semiconductor material.

In re claim 15, Yuan discloses the device of claim 14, wherein the source/drain region of each oxide pillar acts as either a source connection or a drain connection in response to a diretion of operation of the VNROM memory cell.

In re claim 16, Yuan discloses the device of claim 14, wherein each second source/drain region is comprised of N+ conductivity silicon material.

In re claim 19, Yuan discloses the device of claim 17, wherein the first type conductivity is N+ and the substrate is P+ conductivity.

In re claim 20, Yuan discloses the device of claim 17, wherein the first and second gate insulator layers comprise ONO.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8-10, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuan et al. (U.S. Patent No. 6,762,092) in view of Chien et al. (U.S. Patent No. 6,069,042).

In re claim 8, Yuan (esp. Fig. 25A) discloses a semiconductor memory device comprising:

A plurality of oxide pillars each having a source/drain region (449, 451), a trench being formed between each oxide pillar;

A control gate (411) formed between each pair of oxide pillars;

A plurality of program (steering) gates (412), each formed between the control gate and each oxide pillar, each program gate extending along the oxide pillar sidewall; and

A plurality of gate insulator layers (406, ONO), each gate insulator layer formed between each program gate and the adjacent oxide pillar, each gate insulator layer having a structure for trapping at least one charge.

Yuan does not expressly disclose an oxide interpoly layer formed between the control gate and each adjacent program gate. Chien discloses an oxide interpoly layer, which is simply another term for an ONO layer (column 1, lines 37-38) between control and floating (program) gates. It would have been obvious for one skilled in the art at the time of the invention to form this layer of ONO as disclosed by Chien for the device of Yuan for the purpose, for example, of enhancing the charge/discharge operation of the floating gate (column 1, lines 41-65).

In re claim 9, Yuan in view of Chien discloses the device of claim 8, further including a gate insulator formed on the bottom of the trench such that a plurality of charges can be trapped under the control gate in the gate insulator layer.

In re claim 10, Yuan in view of Chien discloses the device of claim 9, wherein the plurality of chares are trapped in a nitride layer of the gate insulator layer under the control gate (Chien; column 1, lines 36-37).

In re claim 13 and 18, Yuan discloses the device of claim 11 and the method of claim 17, further comprising a gate insulator layer on the bottom of each trench, but does not expressly

disclose an oxide interpoly material between each control gate and a structure for storing a plurality of charges under each control gate. Chien discloses an oxide interpoly layer, which is simply another term for an ONO layer (column 1, lines 37-38) between control and floating (program) gates. It would have been obvious for one skilled in the art at the time of the invention to form this layer of ONO as disclosed by Chien for the device of Yuan for the purpose, for example, of enhancing the charge/discharge operation of the floating gate (column 1, lines 41-65).

Allowable Subject Matter

Claims 2, 5, 7, 22-25 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 11/12/04 have been fully considered but they are not persuasive.

a. Applicant is correct in determining that the oxide spacers (407) of Yuan are the interpreted "pillars" of the claimed invention. The claim language of each pair of oxide pillars "having" a source/drain region does not distinguish over Yuan. "Having" in this case, without further structural delineation, can be interpreted to mean "associated with", "with", "in the proximity", etc. Second, nothing in the claims precludes the source/drain regions from being implanted in the substrate.

b. Applicant also asserts that the dielectric layers (406) are outside the channel region and thus would not trap charges. On the contrary, these layers are adjacent the channel regions (415, 416) and, by the nature of their ONO structure, can be expected to trap at least some charge.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

GEORGE ECKERT
PRIMARY EXAMINER